A MICROWAVE PHASE AND GAIN CONTROLLER WITH SEGMENTED-DUAL-GATE MESFETs IN GaAs MMICs

Y.C. Hwang, Y.K. Chen, R.J. Naster
Electronics Laboratory, General Electric Co.
Syracuse, New York 13221

D. Temme
Lincoln Laboratory, Massachusetts Institute of Technology
Lexington, Massachusetts 02173

ABSTRACT

A novel segmented-dual-gate MESFET device which provides precise gain control over broad microwave bandwidth by using prescribed gate-width-ratio is presented. The digitally-controlled precision microwave gain scaler has potential application as an ultra-wide band microwave attenuator or active microwave phase shifter. The design and test results of GaAs MMIC active attenuator and hybrid phase shifter are described.

Introduction

Gallium Arsenide Monolithic Microwave Integrated Circuit (MMIC) technology has matured rapidly during the past few years. Functions usually implemented with passive elements and transmission lines may be replaced by active elements resulting in reduction of chip sizes.

In this paper, a circuit approach utilizing segmented-dual-gate-MESFETs (SDGFETs) to obtain precise gain control is presented. The gain control is achieved by properly scaled gate-width-ratios among the dual-gate MESFETs (DGFETs). Since the gate-width is the least sensitive processing variable, great process resilience is achieved.

Segmented-dual-gate MESFETs

Conventionally, dual-gate MESFETs have been used for gain control [1] by applying an analog voltage on gate #2. The control is non-linear and it is difficult to provide a control voltage with precision and repeatability. While the voltage and impedance applied to the gate #2 are changed, the transfer gain and phase also change depending on the biasing, geometry and process-dependent characteristics of the device. Thus precision cannot be maintained.

In the scheme presented here, we operate the dual gate devices only in the ON/OFF mode by switching the gate #2 bias between two fixed voltage levels, namely saturation and pinch-off, while the bias on gate #1 is kept constant. Several segments of dual-gate MESFETs are integrated together by connecting the gate #1's, sources and drains of each section together as shown in Figure 1. Each dual-gate segment is only operated either fully on or fully off with the input gate bias remaining the same. The layout geometry among dual-gate segments is the same to preserve linear scaling of electrical parameters. The gain of this device is proportional to the collective width of the turned-on segments. By selectively controlling the gate #2's, the gain of this device is programmed exactly. This "scaled-by-width-ratio" can also preserve the relative gain settings against bias and temperature fluctuations as well as process variations.

Modeling of dual-gate FET

It is somewhat difficult to model a dual-gate GaAs MESFET not only because of the physics of its complicated geometry and terminal impedance at gate #2, but also of interacting bias condition [2]. A dual-gate MESFET can be imagined as two single gate MESFET connected in series with the source of the second FET merged with the drain of the first FET. Each FET has two operation regions; the linear and saturated region. The equivalent circuit of the dual-gate MESFET then reflects the state (one out of four) generated from the two serial FETs. That is, different DC bias conditions generate different equivalent circuits for a single DG-MESFET. Since our dual-gate MESFET is only operated in

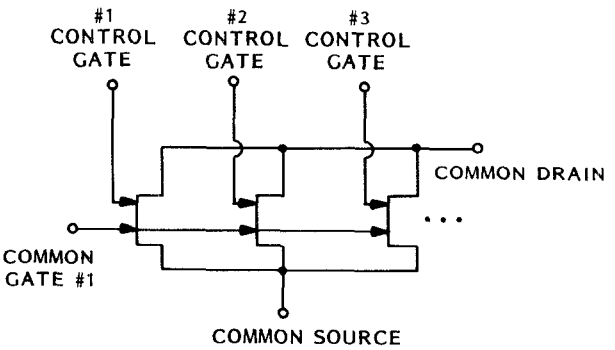
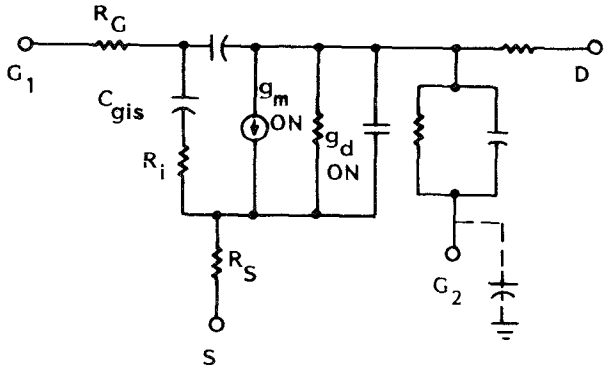
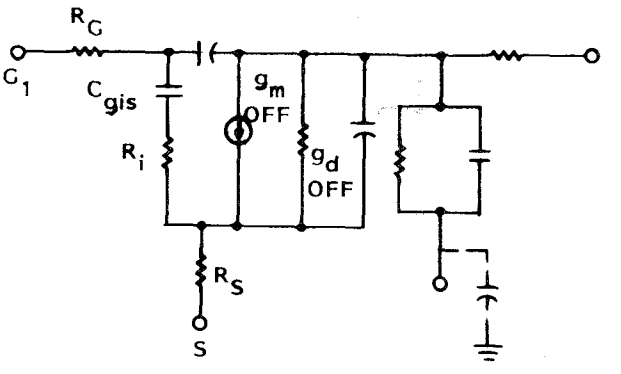


Figure 1. Implementation of a Segmented-Dual-Gate-MESFET Device

This work is supported in part by the Department of the Air Force. The U.S. Government assumes no responsibility for the information presented.



a) ON State



b) OFF State

Figure 2. Simplified Equivalent Circuit Model of a Dual-Gate MESFET Operated in ON/OFF States

either the ON or OFF state, two equivalent circuits for these two biases will be enough.

Figure 2(a) shows the simplified equivalent RF small signal model for MESFET in the ON-state with the second gate represented by a diode (parallel R and C). Figure 2(b) shows the OFF-state equivalent circuit model of the same FET with the same input impedance but different output transconductance and impedance to reflect the pinched-off DG-FET state. The model can be linearly scaled with gate width provided that the geometry and terminal bias voltages and impedances remain the same.

Binary Weighted Scaler

To verify this concept, a binary weighted scaler in the ratio of 1-2-4-8 has been designed and processed on GaAs (Figures 3, 4, and 5). The gate widths of the segments are 50, 100, 200 and 400 μM respectively. The control voltages are fed through 2K ohm resistors on chips. The gates are 1 μM long and separated with 2 μM spacing. The measured performance is shown in Figure 6. The phase and amplitude flatness and tracking over the wide bandwidth is excellent.

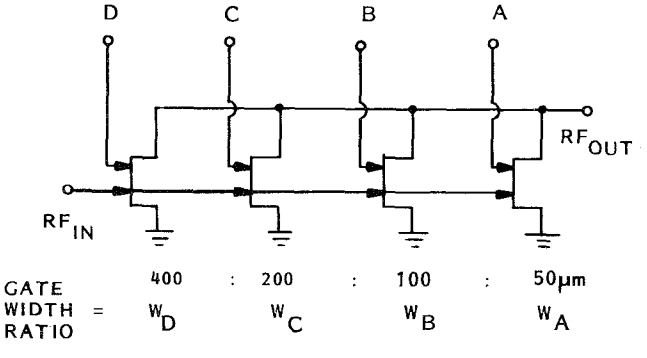


Figure 3. Segmented Dual-Gate MESFETs with Binary Weighting

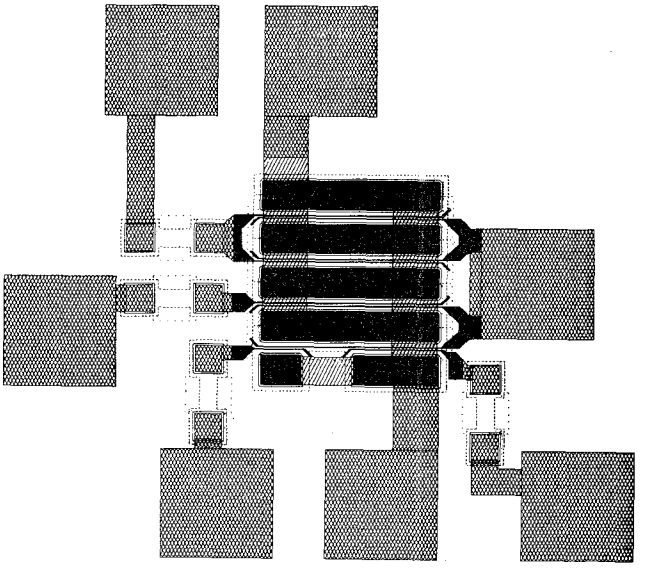


Figure 4. Layout of the 1-2-4-8 Binary Scaler

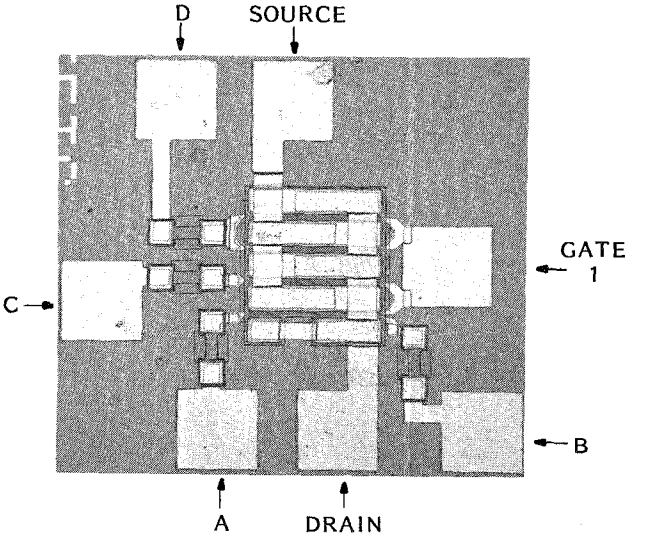
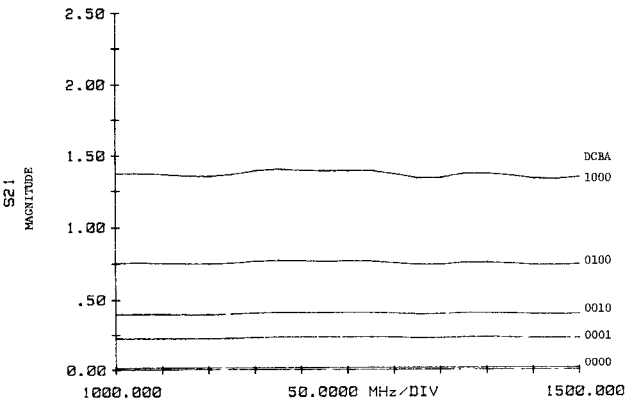
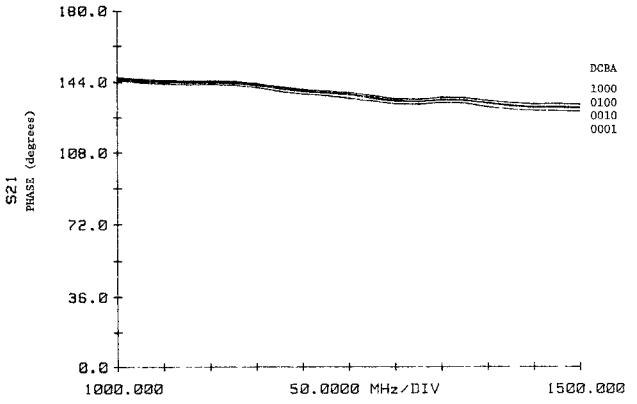


Figure 5. 1-2-4-8 Binary Scaler on Chip



a) Magnitude vs. Frequency



b) Phase vs. Frequency

Figure 6. Magnitude and Phase Characteristics of the 1-2-4-8 Binary Scaler

Microwave sine/cosine function scaler

Another device has been designed to adjust the amplitude for sine function states with settings. The sine function scaler modulates its output signal magnitude by a factor of the sine function value of the designated phasor angle. The cosine function scaler utilizes an identical structure as the sine function scalar except that it is driven by the 90-degree complementary angle of the phasor. Table 1 shows the list of sine and cosine function values for a 4-bit phase shifter. We have adopted this broad band sine function scaler based on the segmented-dual-gate MESFET devices to design a phase shifter which is less sensitive to process variations and whose phase shift is solely determined by the gate width ratios.

Table 1 also shows a sine function for 22.5-degree resolution which is implemented with the "divided-by-13" scheme. From a segmented-dual-gate-MESFET device with three channels of 1:4:8 gate width ratio, values of sine or cosine function at 0, 22.5, 45, 67.5, and 90 degrees can be synthesized by combining the right on and off dual-gate FET segments. Table 2 shows a "divide-by-50" scheme to synthesize a 5-bit phase shifter of 11.25 degrees resolution. Figure 7 shows the photomicrograph of a finished GaAs sine scaler.

Digitally controlled active phase shifter

A phase shifter which consists of a vector modulation scheme and sine/cosine function scalers built on segmented-dual-gate MESFETs is presented. Figure 8 shows the block diagram of a vector modulator. A pair of balanced in-phase (I) and 90-degree (Q) phase vectors are generated from the input RF signal by a 90-degree phase splitter. Since both the sine and cosine scaler will be fabricated on the same MMIC chip, the same insertion gain and phase will be contributed to both the I and Q vectors by the two scalers. The I and Q vectors presented at the output summing point are modulated by the cosine and sine value of the designated phase respectively. The final phase shift is determined solely by the designed width ratios from the two scalers.

TABLE 1

SINE SCALER OF 22.5-DEGREE RESOLUTION FOR 4-BIT PHASE SHIFTER

Angle (degree)	Sine Value	1/13 Approximation	Simulated by control the width of a segmented-dual-gate MESFET device		
			W_{8x}	W_{4x}	W_{1x}
0	0	0/13 (.000)	OFF	OFF	OFF
22.5	.383	5/13 (.384)	OFF	ON	ON
45.0	.707	9/13 (.692)	ON	OFF	ON
67.5	.924	12/13 (.923)	ON	ON	OFF
90.0	1	13/13 (1.000)	ON	ON	ON

TABLE 2

SINE FUNCTION SCALER WITH 11.25° RESOLUTION FOR A 5-BIT PHASE SHIFTER

Angle (degree)	Sine Value	1/50 Approximation	Width control of a segment-dual-gate-MESFET device				
			W_{20x}	W_{14x}	W_{11x}	W_{10x}	W_{5x}
0	0	0/50 (.000)	0	0	0	0	0
11.25	.195	10/50 (.200)	0	0	0	1	0
22.5	.383	19/50 (.380)	0	1	0	0	1
33.75	.556	29/50 (.580)	0	1	0	1	1
45.0	.707	35/50 (.700)	1	0	0	1	1
56.25	.831	41/50 (.820)	1	0	1	1	0
67.50	.924	46.50 (.920)	1	0	1	1	1
78.75	.981	49/50 (.980)	1	1	0	1	1
90.00	1	50/50 (1.000)	1	1	1	0	1

0: segment FET OFF
1: segment FET ON

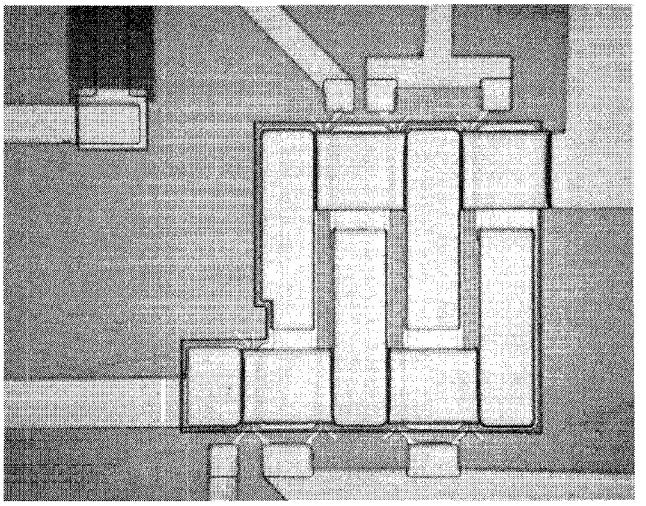


Figure 7. Segmented Dual-Gate MESFETs with 1-4-8 Weighting for Sine Function Scaler

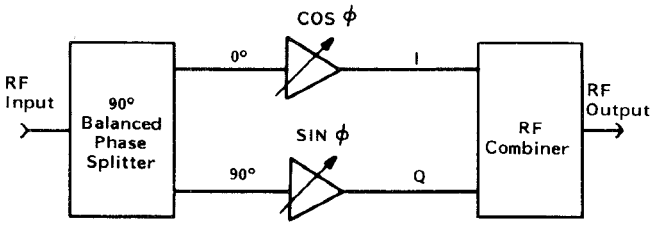


Figure 8. Block Diagram of a Vector Modulator Approach of Microwave Phase Shifter

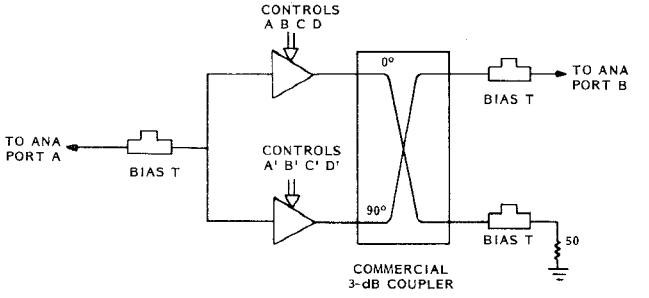


Figure 9. Phase Shifter with the Sine Function Scaler Chip

The phase shifter bandwidth is only limited by the response of the 90-degree phase splitter and the input and output matching circuits connected to it. Since the resultant phase shifts are determined by the turned-on gate width ratios, they are less sensitive to processing variations and the operating environment. The amplitude of the phase shifter is also constant over different phase states and some trimming capability is easy to achieve by fine-tuning the bias on gate #2's.

Figure 9 shows the hybrid test schematic for a 0-90 degree phase shifter that utilizes the vector modulator scheme with the segmented-dual-gate MESFETs

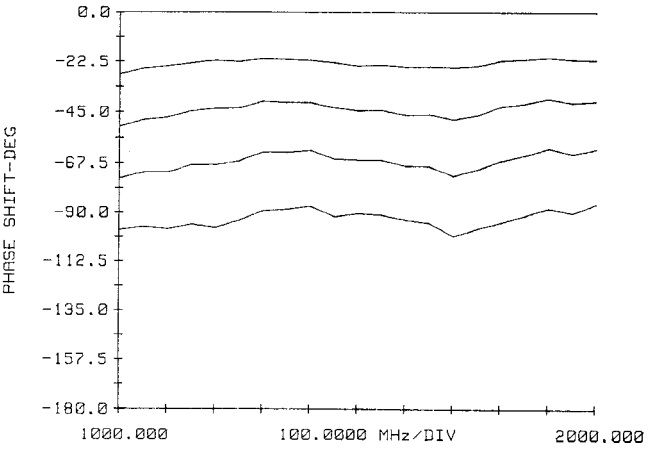


Figure 10. Relative Phase Shift Variations over L-Band

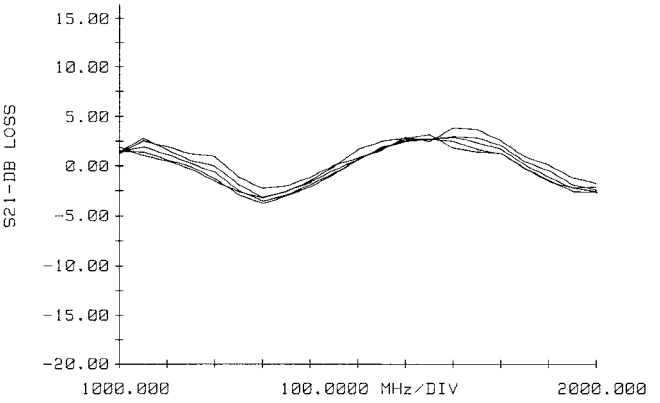


Figure 11. Relative Magnitude Variations over L-Band

shown in Figure 5. Figure 10 shows the phase characteristic of the circuit over the 1000 to 2000 MHz frequency range. The magnitude fluctuation shown in Figure 11 is due mainly to the coupler characteristic.

Active wideband attenuator

If the reference state of a segmented-dual-gate-MESFET device is set such that all segments are biased ON, a specific attenuation can be achieved by turning off a portion of the dual-gate segments. In this case the relative attenuation depends on the width ratio. The "relative" attenuation is independent of any process variations as long as the segments are of the same geometry and they are integrated in such a small area that the fabrication process treats them equally. However, the "insertion" gain of this attenuator will be set by different processing and biasing conditions.

Figure 12 shows the circuit diagram for such an active attenuator. The linear gain S21 of this device can be programmed from 0 to prescribed steps if the gain of a fully turned on device is normalized as unity. In the MMIC format, all contributing channel segments are fabricated in a very close proximity.

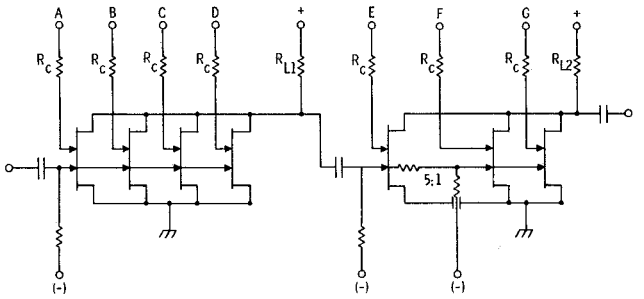


Figure 12. Attenuator with Segmented-Dual-Gate MESFETs

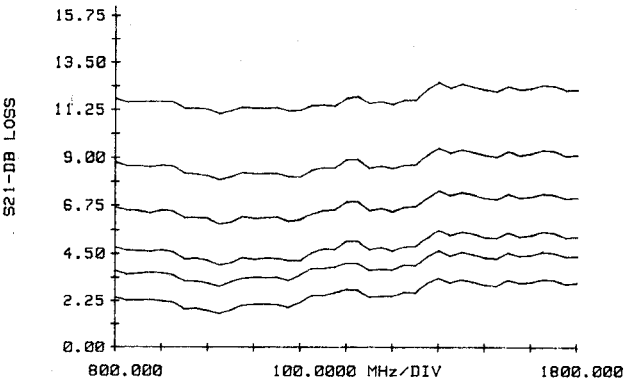


Figure 14. Measurement Result of the Primary Portion of the MMIC Active Attenuator Chip

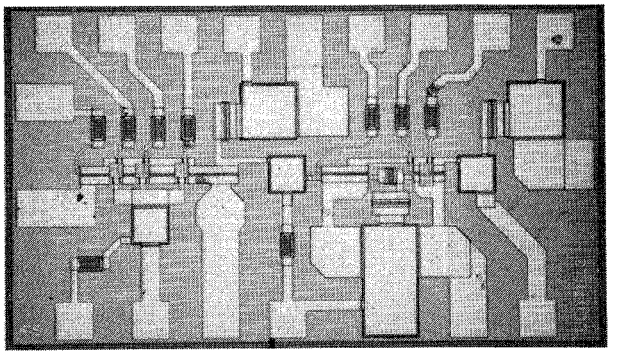


Figure 13. MMIC of the L-Band Attenuator

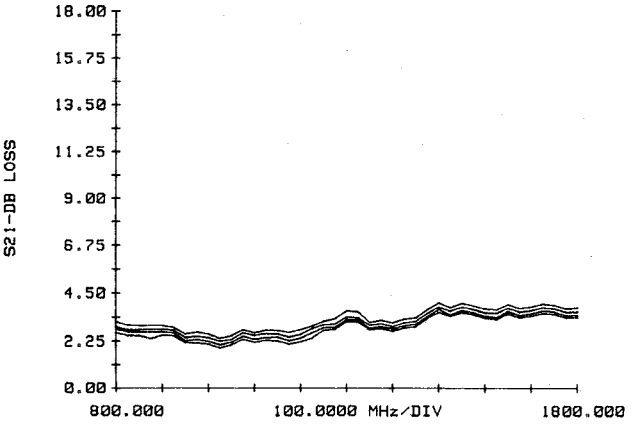


Figure 15. Measurement Result of the Trimming Portion of the MMIC Active Attenuator Chip

Transistor parameters among the dual-gate segments are scaled linearly by the ratio of their width, because they are fabricated under identical processing environments.

However, three major factors need to be considered in order to obtain intended RF gains by linear scaling of the combined width ratios. They are: (1) the loading effect from paralleling DGFETs of finite output impedance; (2) the back-gating effect from the non-ideal substrate, and (3) fringing fields from using DFGETs of short gate width. These non-ideal factors are circumvented by using good material, a set of carefully constructed design rules, and accurate simulations.

The performance for the monolithic attenuator shown in Figure 13 is plotted in Figures 14 and 15. It has a broadband capability from UHF up to 2000 MHz with maximum error within 0.5 dB from the designed primary attenuation settings and 0.2 dB from the designed trimmer settings.

Conclusions

A microwave scaler using a segmented-dual-gate-MESFET with GaAs technology has been presented. It has applications in broadband attenuators and phase shifters. Accurate amplitude control and phase shift control when implemented in a phase vector modulator are possible. By segmenting the gate #2, the need to accurately set in an analog bias on the gate #2 of a continuous dual gate FET is eliminated.

References

[1] Charles A. Liechti, "Performance of Dual-Gate GaAs MESFETs as Gain-Controlled Low Noise Amplifiers and High-Speed Modulators," IEEE, T-MTT, Vol. MTT-23, No. 6, June 1975, pp. 461-469.

[2] C. Tsironis, R. Meierer, "Microwave Wideband Model of GaAs Dual-Gate MESFET," IEEE T-MTT, Vol. MTT-30, No. 3, Mar. 1982.